BUILT-IN SELF-TEST (BIST) ARCHITECTURE HAVING DISTRIBUTED INTERPRETATION AND GENERALIZED COMMAND PROTOCOL

ABSTRACT

A built-in self-test (BIST) architecture having distributed algorithm interpretation is described. The architecture includes three tiers of abstraction: a centralized BIST controller, a set of sequencers, and a set of memory interfaces. The BIST controller stores a set of commands that generically define an algorithm for testing memory modules without regard to the physical characteristics or timing requirements of the memory modules. The sequencers interpret the commands in accordance with a command protocol and generate sequences of memory operations. The memory interfaces apply the memory operations to the memory module in accordance with physical characteristics of the memory module, e.g., by translating address and data signals based on the row-column arrangement of the memory modules to achieve bit patterns described by the commands. The command protocol allows powerful algorithms to be described in an extremely concise manner that may be applied to memory modules having diverse characteristics.